WHAT IS CLAIMED IS:

1. A method of operating a memory circuit, comprising the steps of:

storing a first data word at a first address in a nonvolatile memory circuit;

storing the first address and the first data word in a volatile memory circuit;

applying a first external address to the volatile memory circuit;

comparing the first external address to the first address;

producing the first data word from the volatile memory circuit on a data bus when the first external address matches the first address; and

producing the first data word from the nonvolatile memory circuit on the data bus when the first external address does not match the first address.

2. A method as in claim 1, wherein the nonvolatile memory circuit is a ferroelectric memory circuit.

3. A method as in claim 1, comprising the step of detecting an invalid address in the volatile memory circuit.

4. A method as in claim 1, comprising the step of storing the first external address and the first data word in the volatile memory circuit when the first external address does not match the first address.

5. A method as in claim 1, comprising the steps of:

pointing to an address in the volatile memory circuit with an address pointer;

changing the address pointer when the first external address does not match the first address.

6. A method as in claim 1, comprising the steps of :

applying a second external address to the volatile memory circuit and to the nonvolatile memory circuit;

applying a second data word to the volatile memory circuit and to the nonvolatile memory circuit;

comparing the second external address to the first address;

not changing the first address in the volatile memory circuit when the second external address matches the first address;

storing the second data word in the volatile memory circuit; and

storing the second data word in the nonvolatile memory circuit at the second external address.

7. A method as in claim 1, comprising the step of producing a control signal at the volatile memory circuit in response to the step of comparing, the control signal arranged to control data production by the nonvolatile memory circuit.

8. A method of operating a memory circuit, comprising the steps of:

storing a first data word at a first address in a first memory circuit;

storing the first address and the first data word in a second memory circuit;

enabling the first and second memory circuits;

applying a first external address to the second memory circuit;

comparing the first external address to the first address;

disabling the first memory circuit in response to the step of comparing when the first external address matches the first address;

producing the first data word from the second memory circuit on a data bus when the first external address matches the first address; and

producing the first data word from the first memory circuit on the data bus when the first external address does not match the first address.

9. A method as in claim 8, wherein the first memory circuit is a ferroelectric memory circuit.

10. A method as in claim 8, comprising the step of detecting an invalid address in the second memory circuit.

11. A method as in claim 8, comprising the step of storing the first external address and the first data word in the second memory circuit when the first external address does not match the first address.

12. A method as in claim 8, comprising the steps of:

pointing to an address in the second memory circuit with an address pointer;

changing the address pointer when the first external address does not match the first address.

13. A method as in claim 8, comprising the steps of :

applying a second external address to the first memory circuit and to the second memory circuit;

applying a second data word to the first memory circuit and to the second memory circuit;

comparing the second external address to the first address;

not changing the first address in the second memory circuit when the second external address matches the first address;

changing the first address to the second external address in the second memory circuit when the second external address does not match the first address;

storing the second data word in the second memory circuit; and

storing the second data word in the first memory circuit at the second external address.

14. A method as in claim 8, comprising the step of producing a control signal at the second memory circuit in response to the step of comparing, the control signal arranged to control data production by the first memory circuit.

15. A circuit, comprising:

an address table arranged to store a plurality of addresses and coupled to receive an external address;

a data table coupled to the address table and arranged to store a first plurality of data words, each data word corresponding to a respective address in the address table;

a nonvolatile memory circuit arranged to store a second plurality of data words greater than the first plurality; and

a data terminal coupled to the data table and to the nonvolatile memory circuit.

16. A memory circuit as in claim 15, wherein the nonvolatile memory circuit comprises a plurality of ferroelectric memory cells.

17. A memory circuit as in claim 15, comprising an address table pointer coupled to the address table and arranged to address the address table.

18. A memory circuit as in claim 17, wherein the address table comprises 2^N words and wherein the address table pointer includes more than N bits.

19. A memory circuit as in claim 17, comprising a pulse generating circuit arranged change the address table pointer.

20. A computer system, comprising:

a processor circuit;

a nonvolatile memory circuit arranged to store a first data word at a first address;

a volatile memory circuit arranged to store the first data word and the first address;

a data bus coupled to the processor and the volatile and nonvolatile memory circuits; and

and address bus coupled to the processor and the volatile and nonvolatile memory circuits.

21. A computer system as in claim 20, wherein the nonvolatile memory circuit comprises a plurality of ferroelectric memory cells.

22. A computer system as in claim 20, wherein the nonvolatile memory circuit comprises an address table pointer coupled to the address table and arranged to address the address table.

23. A computer system as in claim 20, wherein the nonvolatile and volatile memory circuits are coupled to receive a system clock signal from the processor.

24. A computer system as in claim 20, wherein the nonvolatile memory circuit is coupled to receive a control signal from the volatile memory circuit, the control signal arranged to control data production from the nonvolatile memory circuit.